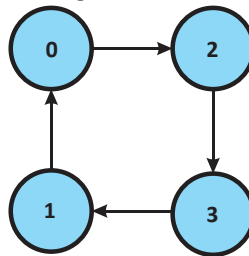


Author Identification Block

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Course: CMSC 2833 – Computer Organization I
CRN: 13097 Autumn 2020
Assignment: a06
Due: October 20, 2020

Scoring block			
Exercise	Maximum	Earned	Explanation
1	3	3	
2	3	3	
3	3	3	
4	3	3	
5	3	3	
Total	15	15	

1. Design a circuit that implements the state diagram shown.



Symbolic State Diagram

- (a) Determine the number of Flip-Flops, assign states, and make a Present-State-Next-State Table.

Solution:

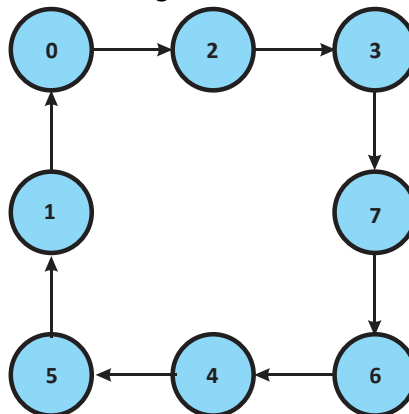
- (b) Produce K-Maps for the next state decoder. Employ D Flip-Flops.

Solution:

- (c) Draw the logic diagram for the circuit.

Solution:

2. Design a circuit that implements the state diagram shown.



Symbolic State Diagram

- (a) Determine the number of Flip-Flops, assign states, and make a Present-State-Next-State Table.

Solution:

- (b) Produce K-Maps for the next state decoder. Employ JK Flip-Flops.

Solution:

- (c) Draw the logic diagram for the circuit.

Solution:

3. Design a circuit that will recognize the sequence 0111. The circuit samples an input line X on each rising-edge of the clock. The circuit raises the output signal $Y = 1$ when the sequence is recognized, otherwise, the output signal is set to zero ($Y = 0$). The circuit recognizes the sequence in any window of four clock pulses.

(a) Draw a block diagram of the circuit.

Solution:

(b) Create a State Diagram for the circuit.

Solution:

(c) Determine the number of Flip-Flops, assign states, and make a Present-State-Next-State Table.

Solution:

(d) Make a Present-State-Next-State Table.

Solution:

(e) Add the Next-State Decoder to the Present-State-Next-state Table using D and JK Flip-Flops..

Solution:

(f) Produce the K-Maps for the Next-State Decoder using D and JK Flip-Flops.

Solution:

(g) Draw the logic diagram of the circuit using the decoder having the fewest gates.

Solution:

4. Design a circuit that will recognize the sequence 110. The circuit samples an input line X on each rising-edge of the clock. The circuit raises the output signal $Y=1$ when the sequence is recognized, otherwise, the output signal is set to zero ($Y=0$). The circuit recognizes the sequence in any window of four clock pulses.

(a) Draw a block diagram of the circuit.

Solution:

(b) Create a State Diagram for the circuit.

Solution:

(c) Determine the number of Flip-Flops, assign states, and make a Present-State-Next-State Table.

Solution:

(d) Make a Present-State-Next-State Table.

Solution:

(e) Add the Next-State Decoder to the Present-State-Next-state Table using D and JK Flip-Flops..

Solution:

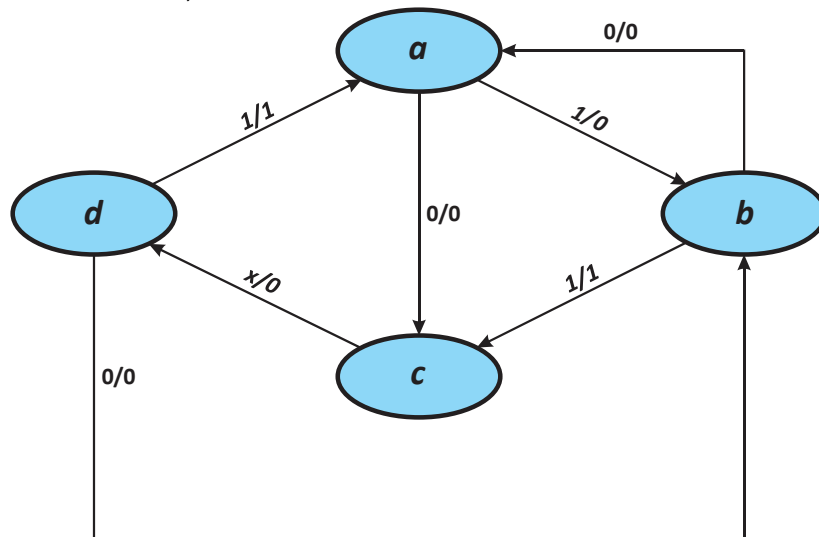
(f) Produce the K-Maps for the Next-State Decoder using D and JK Flip-Flops.

Solution:

(g) Draw the logic diagram of the circuit using the decoder having the fewest gates.

Solution:

5. Design a circuit that implement the state diagram shown. The circuit has one input signal W and one output signal Z . Directed edges that designate state transitions are marked W/Z . Input signals can take on one of three symbols, 1, 0, or x . The symbol x means that the directed edge is really two directed edges, one for $W = 1$, and the other for $W = 0$.



(a) Draw a block diagram of the circuit.

Solution:

(b) Determine the number of Flip-Flops, assign states, and make a Present-State-Next-State Table.

Solution:

(c) Produce the K-Maps for the Next-State Decoder using D and JK Flip-Flops.

Solution:

(d) Draw the logic diagram of the circuit using the decoder having the fewest gates.

Solution: